8-bit MCU with 32K byte Flash, 10 bit A/D and EEPROM

1. Description

The T89C51AC2 is a high performance FLASH version of the 80C51 single chip 8-bit microcontrollers. It contains a 32Kbyte Flash memory block for program and data.

The 32K byte FLASH memory can be programmed either in parallel mode or in serial mode with the ISP capability or with software. The programming voltage is internally generated from the standard V_{CC} pin.

The T89C51AC2 retains all features of the 80C52 with 256 bytes of internal RAM, a 7-source 4-level interrupt controller and three timer/counters.

In addition, the T89C51AC2 has a 10 bit A/D converter, a 2Kbytes Boot Flash memory, 2 Kbyte EEPROM for data, a Programmable Counter Array, an XRAM of 1024 bytes, a Hardware Watchdog Timer and a more versatile serial channel that facilitates multiprocessor communication (EUART).

The fully static design of the T89C51AC2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The T89C51AC2 has 2 software-selectable modes of reduced activity and an 8 bit clock prescaler for further reduction in power consumption. In the idle mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

The added features of the T89C51AC2 make it more powerful for applications that need A/D conversion, pulse width modulation, high speed I/O and counting capabilities such as industrial control, consumer goods, alarms, motor control, ...

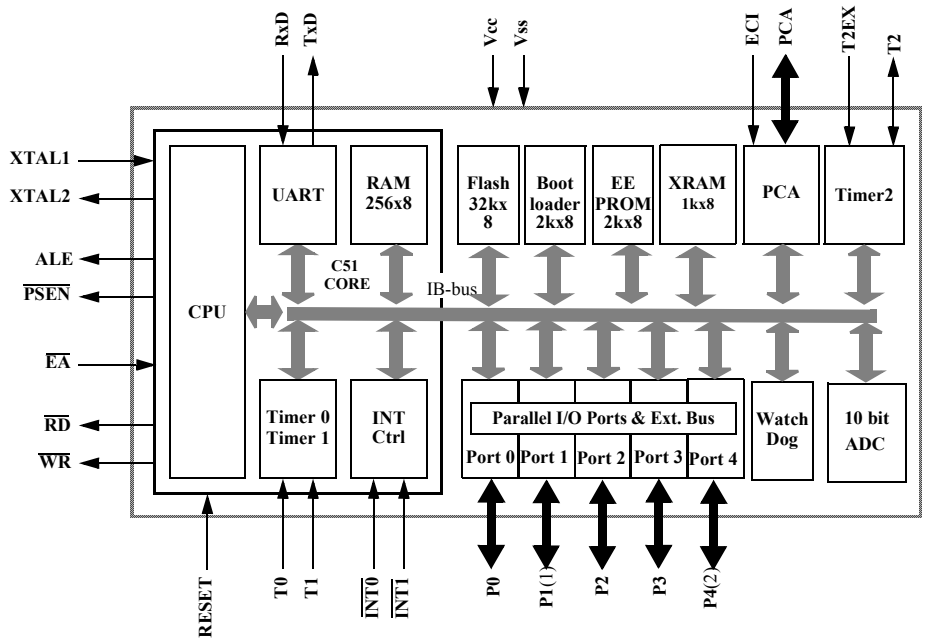
While remaining fully compatible with the 80C52 it offers a superset of this standard microcontroller. In X2 mode a maximum external clock rate of 20 MHz reaches a 300 ns cycle time.

2. Features

- 80C52 core architecture
  - Double Data Pointer
  - 256 bytes of on-chip RAM
- 1Kbytes of on-chip XRAM
- 32 Kbytes of on-chip Flash memory
- 2 Kbytes of on-chip Flash for Bootloader
- 2 Kbytes of on-chip EEPROM
- 14 interrupt sources with 4 priority level
- Three 16-bit timer/counters
- Full duplex Enhanced UART
- High speed architecture
  - 40 MHz in standard mode
  - 20 MHz in X2 mode (6 clocks/machine cycle)
- Five ports: 32 + 2 digital I/O lines
- Programmable Counter Array with 5 16-bit channels :
  - High-speed output
  - Compare / Capture
  - Pulse Width Modulator
  - Watchdog Timer (Channel 4)
- Hardware watchdog timer (One-time enabled with Reset-out)
- A 10-bit resolution analog to digital converter (ADC) with 8 multiplexed inputs
  - 20 microsecond conversion time
  - Two conversion modes
- Asynchronous port reset
- Low EMI (inhibit ALE)
- Power control modes:
  - Idle mode
  - Power down mode
- Power supply: 4.5V to 5.5V
- Temperature range: Industrial (-40 to +85C)
- Packages: VQFP44 1,4 mm, PLCC44, CA-BGA64*
  ** on request*

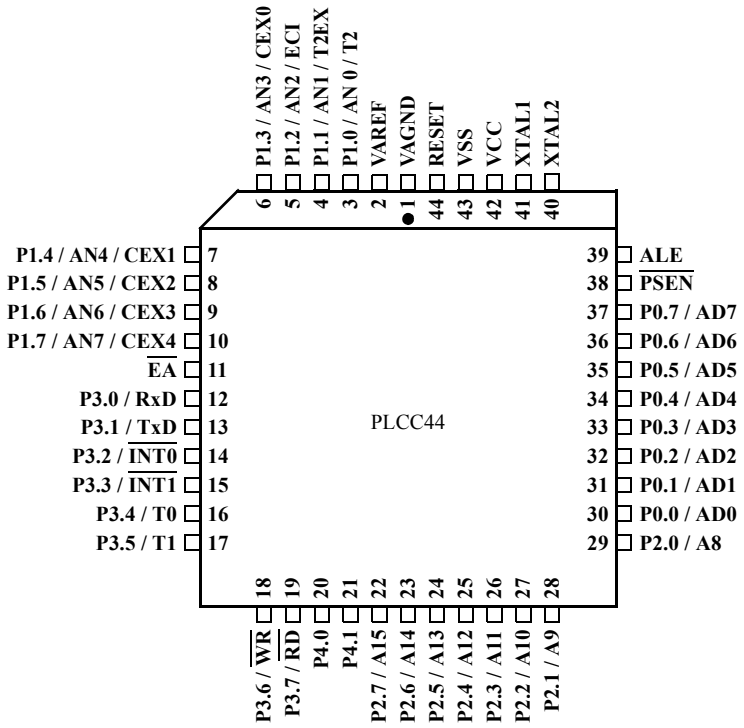
Preliminary

3. Block Diagram



(1): 8 analog Inputs / 8 Digital I/O
(2): 2-bit I/O Port

4. Pin Configuration



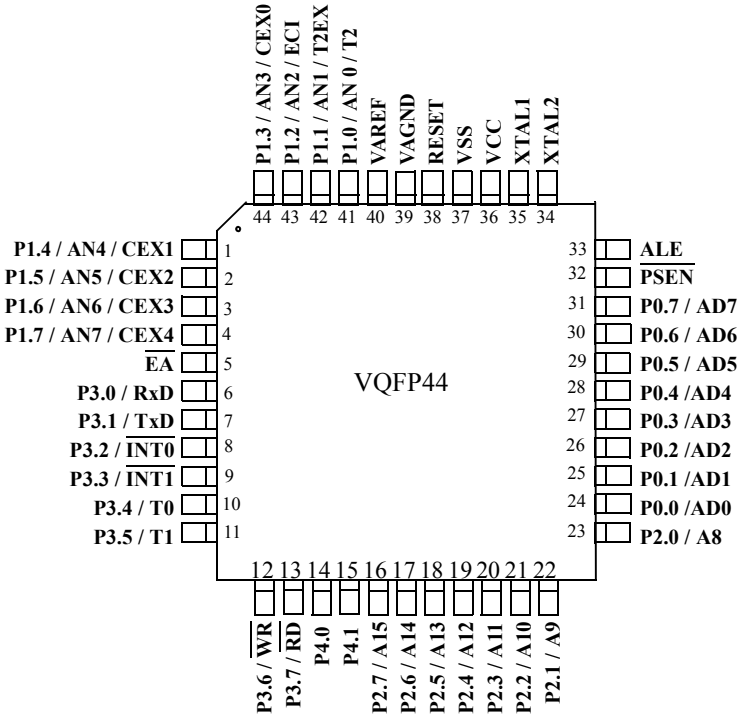


Table 1. Pin Description

Pin Name	Pin Number		Type	Description
	PLCC44	VQFP44		
P0.0-P0.7	30-37	24-31	I/O	**Port 0:** Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pull-ups when emitting 1's. Port 0 also outputs the code bytes during program validation. External pull-ups are required during program verification. In the T89C51AC2 Port 0 can sink or source 5mA. It can drive CMOS inputs without external pull-ups.
P1.0-P1.7	3-10	41-44, 1-4	I/O	**Port 1:** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. Port 1 pins can be used for digital input/output or as analog inputs for the Analog Digital Converter (ADC). Port 1 pins that have 1's written to them are pulled high by the internal pull-up transistors and can be used as inputs in this state. As inputs, Port 1 pins that are being pulled low externally will be the source of current (IIL, on the datasheet) because of the internal pull-ups. Port 1 pins are assigned to be used as analog inputs via the ADCCF register. As a secondary digital function, port 1 contains the Timer 2 external trigger and clock input; the PCA external clock input and the PCA module I/O. Port 1 receives the low-order address byte during FLASH programming and program verification. In the T89C51AC2 Port 1 can sink or source 5mA. It can drive CMOS inputs without external pull-ups.
	3	41	I/O	P1.0 : Input / Output
			I	AN0 : Analog input channel 0
			I	T2 : External clock input for Timer/counter2
	4	42	I/O	P1.1 : Input / Output
			I	AN1 : Analog input channel 1
			I	T2EX : Trigger input for Timer/counter2
	5	43	I/O	P1.2 : Input / Output
			I	AN2 : Analog input channel 2
			I	ECI : PCA external clock input
	6	44	I/O	P1.3 : Input / Output
			I	AN3 : Analog input channel 3
			O	CEX0 : PCA module 0 Entry of input/PWM output
	7	1	I/O	P1.4 : Input / Output
			I	AN4 : Analog input channel 4
			O	CEX1 : PCA module 1 Entry of input/PWM output
	8	2	I/O	P1.5 : Input / Output
			I	AN5 : Analog input channel 5
			O	CEX2 : PCA module 2 Entry of input/PWM output
	9	3	I/O	P1.6 : Input / Output
			I	AN6 : Analog input channel 6
			O	CEX3 : PCA module 3 Entry of input/PWM output
	10	4	I/O	P1.7 : Input / Output
			I	AN7 : Analog input channel 7
			O	CEX4 : PCA module 4 Entry of input/PWM output

Pin Name	Pin Number		Type	Description
	PLCC44	VQFP44		
P2.0:7	29-22	23-16	I/O	**Port 2:** Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled high by the internal pull-ups and can be used as inputs in this state. As inputs, Port 2 pins that are being pulled low externally will be a source of current (IIL, on the datasheet) because of the internal pull-ups. Port 2 emits the high-order address byte during accesses to the external Program Memory and during accesses to external Data Memory that uses 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 transmits the contents of the P2 special function register. It also receives high-order addresses and control signals during program validation. In the T89C51AC2 Port 2 can sink or source 5mA. It can drive CMOS inputs without external pull-ups.
P3.0 - P3.7	12-19	6-13	I/O	**Port 3:** Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled high by the internal pull-up transistors and can be used as inputs in this state. As inputs, Port 3 pins that are being pulled low externally will be a source of current (IIL, on the datasheet) because of the internal pull-ups. The output latch corresponding to a secondary function must be programmed to one for that function to operate (except for TxD and $\overline{WR}$). In the T89C51AC2 Port 3 can sink or source 5mA. It can drive CMOS inputs without external pull-ups. The secondary functions are assigned to the pins of port 3 as follows:
	12	6	I/O	P3.0 : Input / Output
			I	Rxd : Receiver data input (asynchronous) or data input/output (synchronous) of the serial interface
	13	7	I/O	P3.1 : Input / Output
			O	Txd : Transmitter data output (asynchronous) or clock output (synchronous) of the serial interface
	14	8	I/O	P3.2 : Input / Output
			I	$\overline{INT0}$: External interrupt 0 input / timer 0 gate control input
	15	9	I/O	P3.3 : Input / Output
			I	$\overline{INT1}$: External interrupt 1 input / timer 1 gate control input
	16	10	I/O	P3.4 : Input / Output
			I	T0: Timer 0 counter input
	17	11	I/O	P3.5 : Input / Output
			I	T1: Timer 1 counter input
	18	12	I/O	P3.6 : Input / Output
			O	$\overline{WR}$: External Data Memory write strobe; latches the data byte from port 0 into the external data memory
	19	13	I/O	P3.7 : Input / Output
			O	$\overline{RD}$: External Data Memory read strobe; Enables the external data memory. In the T89C51AC2 Port 3 can sink or source 5mA. It can drive CMOS inputs without external pull-ups.
P4.0-P4.1			I/O	**Port 4:** Is an 2-bit bi-directional I/O port with internal pull-ups. Port 4 pins that have 1's written to them are pulled high by the internal pull-ups and can be used as inputs in this state. As inputs, Port 4 pins that are being pulled low externally will be a source of current (IIL, on the datasheet) because of the internal pull-up transistor.

Pin Name	Pin Number		Type	Description
	PLCC44	VQFP44		
RESET	44	38	I/O	**Reset:** A high level on this pin during two machine cycles while the oscillator is running resets the device. An internal pull-down resistor to VSS permits power-on reset using only an external capacitor to VCC.
ALE	39	33	O	**ALE:** An Address Latch Enable output for latching the low byte of the address during accesses to the external memory. The ALE is activated every 1/6 oscillator periods (1/3 in X2 mode) except during an external data memory access. When instructions are executed from an internal FLASH ($\overline{EA}$ = 1), ALE generation can be disabled by the software.
$\overline{PSEN}$	38	32	O	**$\overline{PSEN}$:** The Program Store Enable output is a control signal that enables the external program memory of the bus during external fetch operations. It is activated twice each machine cycle during fetches from the external program memory. (However, when executing outside of the external program memory two activations of PSEN are skipped during each access to the external Data memory). The PSEN is not activated during fetches from the internal data memory.
$\overline{EA}$	11	5	I	**$\overline{EA}$:** When External Access is held at the high level, instructions are fetched from the internal FLASH when the program counter is less then 8000H. When held at the low level, T89C51AC2 fetches all instructions from the external program memory.
XTAL1	41	35	I	**XTAL1:** Input of the inverting oscillator amplifier and input of the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. To operate above a frequency of 16 MHz, a duty cycle of 50% should be maintained.
XTAL2	40	34	O	**XTAL2:** Output from the inverting oscillator amplifier.
VAGND	1	39	I	**Reference Ground for ADC**
VCC	42	36	I	**Supply voltage during normal, idle, and power-down operation.**
VSS	43	37	I	**Circuit ground potential**.
VAREF	2	40	I	**Reference Voltage for ADC**